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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,412	10/31/2003	Josephus C. Ebergen	SUN-P9550	2088

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EXAMINER	
COONEY, ADAM A	

ART UNIT	PAPER NUMBER
2444	

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02/18/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,412	EBERGEN ET AL.	
	Examiner	Art Unit	
	ADAM COONEY	2444	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/05/2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/05/2010 has been entered.

Response to Arguments

2. Applicant's arguments, see pages 7 and 8, with respect to the rejection of claims 1, 11 and 20 under 35 U.S.C. 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Blanc et al. (U.S. 6,606,300 B1). Applicant states that Orsic fails to teach "*a transmitter in the plurality of transmitters is coupled with an output of an AND gate, a first input of the AND gate is asserted when the transmitter is allowed to transmit based on the presence of the token, a second input of the AND gate is asserted when the receiver is ready to receive from the transmitter, and the transmitter is allowed to transmit when the output of the AND gate is asserted*". The examiner submits that Orsic in combination with Blanc teaches said limitation. Blanc teaches a flow control process for a switching system where an AND gate that receives inputs, such as a signal associated with the possibility of transmitting a cell and a signal associated with authorizing a positive gate signal, can deliver a positive GRANT signal (see

Blanc column 39 lines 25-60). It would be obvious to one of ordinary skill in the art to combined Blanc's teaching with Orsic because Orsic teaches a logic circuit receives a signal from a flip-flop indicating the presence of a e-bit stored and a signal from the output controller (receiver) indicating whether its busy or not and then outputs a grant signal to the input controller (transmitter) (see Orsic column 5 lines 37-53, column 6 lines 15-18 and Figure 2; item 108 Flip Flop, item 111 Logic Circuit and item 104-1 B-line). Since the logic circuit, as taught by Orsic, receives two input signals and then outputs a signal associated with the two input signals, it would be obvious that an AND gate would be implemented in or as the logic circuit, as taught by Blanc, because as known an AND gate is a digital logic gate that implements logical conjunction and therefore can be construed as a logic circuit. Therefore, Orsic in combination with Blanc teaches the amended limitation " *a transmitter in the plurality of transmitters is coupled with an output of an AND gate, a first input of the AND gate is asserted when the transmitter is allowed to transmit based on the presence of the token, a second input of the AND gate is asserted when the receiver is ready to receive from the transmitter, and the transmitter is allowed to transmit when the output of the AND gate is asserted*", as shown in the rejection below. The examiner suggests that the applicant should look in the specification to possibly further define the claims. One example may be in paragraph 0063 of the specification where it states the "*controller can define a new clearance-to-send signal for a transmitter as the logical AND* ***of the old clearance-to-send signal*** *for the transmitter and the flow control signal of the receiver*", this seems to imply that one of the inputs to the AND gate must be a previous grant/clearance-to-send signal. As such, applicant may want to look into incorporating this feature into the claim language.

3. Applicant's arguments, see page 9, with respect to the rejection of claims 2-10 and 12-19 under 35 U.S.C 102(b) have been fully considered but are moot in view of the new ground(s) of rejection and also due to claims 2-10 and 12-19 dependency upon rejected independent claims 1 and 11.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Orsic (U.S. 4,817,082) in view of Blanc et al. (U.S. 6,606,300 B1).

4. Regarding independent claim 1, Orsic teaches Orsic teaches a system for regulating communications between a plurality of transmitters (input controllers) and a receiver (output controllers) (see column 3 lines 48-53 and Figure 1; input controller transmits a packet to output controller, therefore input controller is the transmitter and output controller is the receiver), comprising: a plurality of cells (see Figure 1; crosspoint elements, i.e. 107-11 and 107-21), wherein each cell controls communications from a transmitter in the plurality of transmitters to the receiver; wherein the plurality of cells are arranged in a token ring (control ring) that regulates communications from the plurality of transmitters to the receiver; and wherein the presence of a token within a token ring cell indicates that the corresponding transmitter may communicate with the receiver (see column 2 lines 9-35, column 4 lines 16-20 and Figure 1; an

array of crosspoint elements each associated with one of the input means and one of the output means, each crosspoint element is associated with its own control ring, the control mechanism is efficient in enabling packet transmission, further each crosspoint element is responsive to a token for switching information from its associated input means to its associated output means). Although Orsic teaches a signal based on the presence of a token (e-bit) and a signal indicating the receiver is ready to receive from the transmitter (see Orsic column 5 lines 37-53, column 6 lines 15-18 and Figure 2; item 108 Flip Flop, item 111 Logic Circuit and item 104-1 B-line) it does not teach a transmitter in the plurality of transmitters is coupled with an output of an AND gate, a first input of the AND gate is asserted when the transmitter is allowed to transmit based on the presence of the token, a second input of the AND gate is asserted when the receiver is ready to receive from the transmitter, and the transmitter is allowed to transmit when the output of the AND gate is asserted. However, Blanc does teach such a limitation. According to Blanc, a flow control process for a switching system teaches an AND gate that receives inputs, such as a signal associated with the possibility of transmitting a cell and a signal associated with authorizing a positive gate signal, can deliver a positive GRANT signal (see Blanc column 39 lines 25-60). Therefore, it would have been obvious to a person of ordinary skill in the art to have combined Blanc's teaching of an AND gate that receives two input signals and outputs a signal with Orsic's teaching of a logic circuit that receives a signal from a flip-flop indicating the presence of a e-bit stored and a signal from the output controller (receiver) indicating whether its busy or not and then outputs a grant signal to the input controller (see Orsic column 5 lines 37-53, column 6 lines 15-18 and Figure 2; item 108 Flip Flop, item 111 Logic Circuit and item 104-

1 B-line) because as known an AND gate is a digital logic gate that implements logical conjunction and therefore can be construed as a logic circuit.

5. Regarding claim 2, Orsic and Blanc teach all the limitations of independent claim 1, as discussed above. Further, Orsic teaches a plurality of receivers (see Figure 1); and a plurality of token rings (see column 2 lines 32-33 and Figure 1), wherein each token ring passes a corresponding token among token ring cells that control communications from the plurality of transmitters to a receiver corresponding to the token ring (see column 2 lines 13-29, column 3 lines 34-37 and column 4 lines 16-20).

6. Regarding claim 3, Orsic and Blanc teach all the limitations of claim 2, as discussed above. Further, Orsic teaches wherein the plurality of cells are arranged in a grid (array) wherein a row corresponds to a transmitter and a column corresponds to a receiver (see column 2 lines 25-29 and Figure 1).

7. Regarding claim 4, Orsic and Blanc teach all the limitations of independent claim 1, as discussed above. Further, Orsic teaches wherein the communications can include one of: an electrical signal; a mechanical signal; and an optical signal (see column 3 lines 52-58 and Figure 1, it is inherent that when using bus lines, i.e. R and G lines, that an electrical signal is used).

8. Regarding clam 5, Orsic and Blanc teach all the limitations of independent claim 1, as discussed above. Further, Orsic teaches wherein each cell is configured to receive a request signal from a corresponding transmitter, and in response to the request signal, is configured to issue an acknowledgement signal (grant signal) to the corresponding transmitter which allows the corresponding transmitter to begin transmitting if the cell has the token (see column 3 lines 48-68 through column 4 lines 1-6 and 16-20, also column 5 lines 12-26).

9. Regarding claim 6, Orsic and Blanc teach all the limitations of claim 5, as discussed above. Further, Orsic teaches wherein each transmitter further comprises a reset mechanism that is configured to release the clearance to communicate with the receiver by resetting the request signal (see column 4 lines 6-8 and column 5 lines 27-30; once transmission of the packet is complete the input controller "resets" by applying a low signal to the R line of the bus).

10. Regarding claim 7, Orsic and Blanc teach all the limitations of claim 6, as discussed above. Further, Orsic teaches wherein the system further comprises an acknowledgement mechanism configured to confirm the release of the clearance by resetting the acknowledgement signal (see column 4 lines 9-13 and column 5 lines 30-32; the system "confirms the release" by the crosspoint element removing the grant signal from the G line of the bus).

11. Regarding claim 8, Orsic and Blanc teach all the limitations of independent claim 1, as discussed above. Further, Orsic teaches an initialization mechanism configured to initialize the single token in the token ring (see column 3 lines 34-35 and column 4 lines 67-68 through column 5 lines 1-4; generates a new "token", E-bit, therefore initializing the E-bit).

12. Regarding claim 9, Orsic and Blanc teach all the limitations of independent claim 1, as discussed above. Further, Orsic teaches wherein the system operates asynchronously (see column 5 lines 12-34; input controller requests, waits for and receives grant signal, then transmits packet, therefore asynchronous because it is not simultaneous).

13. Regarding claim 10, Orsic and Blanc teach all the limitations of independent claim 1, as discussed above. Further, Orsic teaches wherein the system additionally comprises a flow control mechanism configured to selectively limit the communications from the transmitter to the

receiver at the request of the receiver (see column 6 lines 28-36; "receiver"/output controller provides flow control and applies a busy signal to stop the flow of packets).

14. Regarding independent claim 11, Orsic teaches a method for regulating communications between a plurality of transmitters (input means/input controllers) and a receiver (output means/output controllers) (see column 3 lines 48-53 and Figure 1, i.e. 101-1 and 102-1; input controller transmits a packet to output controller, therefore input controller is the transmitter and output controller is the receiver), comprising: receiving a request signal from a transmitter at a cell (crosspoint element) in a plurality of cells requesting to communicate with the receiver (see column 3 lines 52-62, column 5 lines 16-22 and column 6 lines 3-7); wherein the plurality of cells are arranged in a token ring (control ring) that regulates communications from the plurality of transmitters to the receiver (see column 2 lines 11-24 and Figure 1); and in response to the request signal, issuing an acknowledgement signal (grant signal) to the transmitter which allows the transmitter to begin transmitting if the presence of a token is detected within the cell (see column 3 lines 48-68 through column 4 lines 1-6 and 16-20, also column 5 lines 12-26). Although Orsic teaches a signal based on the presence of a token (e-bit) and a signal indicating the receiver is ready to receive from the transmitter (see Orsic column 5 lines 37-53, column 6 lines 15-18 and Figure 2; item 108 Flip Flop, item 111 Logic Circuit and item 104-1 B-line) it does not teach a transmitter in the plurality of transmitters is coupled with an output of an AND gate, a first input of the AND gate is asserted when the transmitter is allowed to transmit based on the presence of the token, a second input of the AND gate is asserted when the receiver is ready to receive from the transmitter, and the transmitter is allowed to transmit when the output of the AND gate is asserted. However, Blanc does teach such a limitation. According to Blanc,

a flow control process for a switching system teaches an AND gate that receives inputs, such as a signal associated with the possibility of transmitting a cell and a signal associated with authorizing a positive gate signal, can deliver a positive GRANT signal (see Blanc column 39 lines 25-60). Therefore, it would have been obvious to a person of ordinary skill in the art to have combined Blanc's teaching of an AND gate that receives two input signals and outputs a signal with Orsic's teaching of a logic circuit that receives a signal from a flip-flop indicating the presence of a e-bit stored and a signal from the output controller (receiver) indicating whether its busy or not and then outputs a grant signal to the input controller (see Orsic column 5 lines 37-53, column 6 lines 15-18 and Figure 2; item 108 Flip Flop, item 111 Logic Circuit and item 104-1 B-line) because as known an AND gate is a digital logic gate that implements logical conjunction and therefore can be construed as a logic circuit.

15. Regarding claim 12, Orsic and Blanc teach all the limitations of independent claim 11, as discussed above. Further, Orsic teaches wherein the plurality of cells include a plurality of token rings (see column 2 lines 32-33 and Figure 1), wherein each token ring passes a corresponding token among token ring cells that control communications from the plurality of transmitters to a receiver corresponding to the token ring (see column 2 lines 13-29, column 3 lines 34-37 and column 4 lines 16-20).

16. Regarding claim 13, Orsic and Blanc teach all the limitations of independent claim 11, as discussed above. Further, Orsic teaches wherein a plurality of cells that regulate communications between the transmitters and receivers are arranged in a grid (array) wherein a row corresponds to a transmitter and a column corresponds to a receiver (see column 2 lines 25-29 and Figure 1).

17. Regarding claim 14, Orsic and Blanc teach all the limitations of independent claim 11, as discussed above. Further, Orsic teaches wherein the communications can include one of: an electrical signal; a mechanical signal; and an optical signal (see column 3 lines 52-58 and Figure 1, it is inherent that using bus lines, i.e. R and G lines, that an electrical signal is used).

18. Regarding claim 15, Orsic and Blanc teach all the limitations of independent claim 11, as discussed above. Further, Orsic teaches revoking the permission for the transmitter to communicate with the receiver when the transmitter resets the request signal (see column 4 lines 6-8 and column 5 lines 27-32).

19. Regarding claim 16, Orsic and Blanc teach all the limitations of claim 15, as discussed above. Further, Orsic teaches resetting the acknowledgement signal to confirm the revocation of the permission for the transmitter to communicate with the receiver (see column 4 lines 9-13 and column 5 lines 30-32).

20. Regarding claim 17, Orsic and Blanc teach all the limitations of independent claim 11, as discussed above. Further, Orsic teaches initializing the token in the token ring (see column 3 lines 34-35 and column 4 lines 67-68 through column 5 lines 1-4).

21. Regarding claim 18, Orsic and Blanc teach all the limitations of independent claim 11, as discussed above. Further, Orsic teaches wherein the system operates asynchronously (see column 5 lines 12-34; input controller requests, waits for and receives grant signal, then transmits packet, therefore asynchronous because it is not simultaneous).

22. Regarding claim 19, Orsic and Blanc teach all the limitations of independent claim 11, as discussed above. Further, Orsic teaches controlling the flow of communications by selectively limiting the communications from the transmitter to the receiver at the request of the receiver

(see column 6 lines 28-36; "receiver"/output controller provides flow control and applies a busy signal to stop the flow of packets).

23. Regarding independent claim 20, Orsic teaches a multi-processor system, comprising: a plurality of processors (see column 3 lines 1-9 and Figure 1, i.e. 11 and 21; input devices and output devices include terminal equipment, therefore the terminals are the processors); a plurality of transmitters (input controllers) associated with the processors; a plurality of receivers (output controllers) associated with the plurality of processors (see column 3 lines 48-53 and Figure 1; input controller transmits a packet to output controller, therefore input controller is the transmitter and output controller is the receiver); a plurality of cells (see Figure 1; crosspoint elements, i.e. 107-11 and 107-21), wherein each cell controls communications from a transmitter in the plurality of transmitters to a receiver; wherein the plurality of cells are arranged in a token ring (control ring) that regulates communications from the plurality of transmitters to a receiver; and wherein the presence of a token within a token ring cell indicates that the corresponding transmitter may communicate with the receiver (see column 2 lines 9-35, column 4 lines 16-20 and Figure 1; an array of crosspoint elements each associated with one of the input means and one of the output means, each crosspoint element is associated with its own control ring, the control mechanism is efficient in enabling packet transmission, further each crosspoint element is responsive to a token for switching information from its associated input means to its associated output means). Although Orsic teaches a signal based on the presence of a token (e-bit) and a signal indicating the receiver is ready to receive from the transmitter (see Orsic column 5 lines 37-53, column 6 lines 15-18 and Figure 2; item 108 Flip Flop, item 111 Logic Circuit and item 104-1 B-line) it does not teach a transmitter in the plurality of transmitters is coupled with

an output of an AND gate, a first input of the AND gate is asserted when the transmitter is allowed to transmit based on the presence of the token, a second input of the AND gate is asserted when the receiver is ready to receive from the transmitter, and the transmitter is allowed to transmit when the output of the AND gate is asserted. However, Blanc does teach such a limitation. According to Blanc, a flow control process for a switching system teaches an AND gate that receives inputs, such as a signal associated with the possibility of transmitting a cell and a signal associated with authorizing a positive gate signal, can deliver a positive GRANT signal (see Blanc column 39 lines 25-60). Therefore, it would have been obvious to a person of ordinary skill in the art to have combined Blanc's teaching of an AND gate that receives two input signals and outputs a signal with Orsic's teaching of a logic circuit that receives a signal from a flip-flop indicating the presence of a e-bit stored and a signal from the output controller (receiver) indicating whether its busy or not and then outputs a grant signal to the input controller (see Orsic column 5 lines 37-53, column 6 lines 15-18 and Figure 2; item 108 Flip Flop, item 111 Logic Circuit and item 104-1 B-line) because as known an AND gate is a digital logic gate that implements logical conjunction and therefore can be construed as a logic circuit.

Conclusion

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ADAM COONEY whose telephone number is (571)270-5653. The examiner can normally be reached on Monday-Thursday and every other Friday from 730AM-5PM..

25. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William C. Vaughn can be reached on 571-272-3922. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

26. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. C./
Examiner, Art Unit 2444
2/11/2010

/William C. Vaughn, Jr./

Supervisory Patent Examiner, Art Unit 2444